Instructor: Dr. Jing-Chiou Liou  
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Class Room: Tech. H101
Class Hours: Tuesday 17:00 – 22:30
Office Hours: Monday – Thursday. Details provided separately.
Instruction Method: Lecture & Lab.

Textbook:
PowerPoint slides will be used in class.

Grading: Homework (5+1) 20% Midterm 25% Final 25% Lab. (10 reports) 30%

Course Description & Objectives:
This course is a study of digital circuits and systems. Topics covered are: number systems, Boolean algebra, logic gates, Flip-Flops, counters, memory, combinational circuits, synchronous and asynchronous sequential systems.

Upon completion of the course, we will have a fully understanding of the binary systems that are the fundamental blocks of modern digital systems. We will also be capable of performing analysis and design of digital systems that are currently used in communication, business transactions, traffic control, space guidance, medical instruments, the Internet, and many other commercial, industrial, and scientific enterprises.

Homework Assignments (HAs) and Lab. Report (LRs) submission policy:
- Students are expected to submit HA and/or LR in the following week of the session, unless is mentioned otherwise.
- Late submission is allowed for up to a week delay, with a 10% deduction in grade.

Important University Dates:
9/9/09: Last day to withdraw w/ 100% refund  
9/16/09: Last day to withdraw w/ 75% refund

Academic Integrity Policy: http://www.kean.edu/forms/AcademicIntegrity.pdf
Tutoring and learning Support services: http://www.kean.edu/~castutor
Schedule:
9/8: Course Overview and Number systems.
    Lab Introduction: Procedures/Safety
9/22: Chapter 1: Digital Systems and Binary Numbers.
    Chapter 11-2: Experiment 1 Binary and Decimal Number
    Chapter 11-3: Experiment 2 Digital Logic Gates
10/6: Chapter 3: Gate-Level Minimization.
    Chapter 11-4: Experiment 3 Simplification of Boolean Functions
10/13: Chapter 4: Combinational Logic (I).
    Chapter 11-5: Experiment 4 Combinational Circuits
    Chapter 11-6: Experiment 5 Code Converters
10/20: Chapter 4: Combinational Logic (II).
    Chapter 11-7: Experiment 6 Design with Multiplexers
    Chapter 11-8: Experiment 7 Adders and Subtractors
10/27: Midterm Exam.
11/3: Chapter 5: Synchronous Sequential Logic (I).
    Chapter 11-9: Experiment 8 Flip-Flops
11/10: Chapter 5: Synchronous Sequential Logic (II).
    Chapter 11-10: Experiment 9 Sequential Circuits
11/17: Chapter 6: Registers and Counters.
    Chapter 11-11: Experiment 10 Counters
    Chapter 11-12: Experiment 11 Shift Registers
11/24: Chapter 7: Memory and Programmable Logic.
    Chapter 11-13: Experiment 12 Serial Addition
    Chapter 11-14: Experiment 13 Memory Unit
12/1: Chapter 9: Asynchronous Sequential Logic.
    Chapter 11-16: Experiment 15 Clock Pulse Generator
12/8: Chapter 9: Asynchronous Sequential Logic.
    Chapter 11-19: Experiment 18 Asynchronous Sequential Circuits
12/15: Final Exam.